UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,280	03/25/2004	Tatsunori Kanai	251119US2SRD	5189

22850 7590 11/02/2007

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LEE, KWOK W	

ART UNIT	PAPER NUMBER
4113	

NOTIFICATION DATE	DELIVERY MODE
11/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/808,280	KANAI ET AL.	
	Examiner	Art Unit	
	Kwok Wing Lee	4113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :8/9/04, 10/18/04, 12/8/04, 12/19/2005, 8/22/06, 9/6/06.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) filed on 08/09/2004, 10/18/2004, 12/08/2004, 12/19/2005, 08/22/2006 and 09/06/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 7-9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A "program" is not a "process, machine, manufacture or composition of matter." The claimed "program" invention is merely software per se and cannot be construed to be any of the statutory patentable subject matters.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kartalopoulos (US 5,590,323).

With respect to claims 1 and 7, Kartalopoulos teaches a method or a program, respectively, performing a real-time operation including a combination of a plurality of tasks, the method or program comprising: inputting structural description information (See Matrix table in figure 1) and a plurality of programs (Column 1, lines 55-57) describing procedures corresponding to the tasks (it is inherent that programs describe a series of procedures that correspond to a task), the structural description information indicating a relationship in input/output between the programs (Column 5, line 63-column 6, line 7 and column 6, line 43-46, note that communication and the exchange of results of one program with another indicates that there is an input/output relationship between them) and including cost information (Column 6, lines 15-30) concerning a time required for executing each of the programs; determining an execution start timing and execution term (Column 5, line 66-column 6, line 14 and see Matrix table in figure 1) of each of a plurality of threads (it is inherent that sets of tasks are assigned to individual threads to execute) for execution of the programs based on the structural description information; and performing a scheduling operation (Column 6, lines 39-46 and see Matrix table of figure 1) of assigning the threads to one or more processors according to a result of the determining.

With respect to claims 2 and 8, Kartalopoulos teaches the method or program according to claim 1 and 7, respectively, wherein the structural description information includes coupling attribute information (Column 6, lines 1-7, where the coupling attribute information is the dependent task relationship represented by the Matrix table as shown in figure 1) indicative of a coupling attribute between the programs, and the method

further comprises selecting a tightly coupled thread group from among the plurality of threads based on the coupling attribute information (Column 5, line 66-column 6, line 3), the tightly coupled thread group including a set of tightly coupled threads running in cooperation with each other (Column 6, lines 1-6 and see Matrix table in figure 1), and determining several processors of the processors, to which the tightly coupled threads are to be assigned (Column 6, lines 39-44), to simultaneously execute the tightly coupled threads by the several processors (See Matrix table, as explained by Column 6, lines 39-44, note that each row corresponds to one microprocessor and as shown in the table and each column indicates simultaneous tasks to be processed in a slotted time interval), the several processors being equal in number to the tightly coupled threads (Column 6, lines 39-42).

With respect to claims 3 and 9, Kartalopoulos teaches the method or program according to claim 2 and 8, respectively, wherein each of the several processors includes a local memory (Column 2, lines 26-32), and the method further comprises mapping the local memory of one of the several processors, which executes one of the tightly coupled threads, in part of an effective address space of another of the tightly coupled threads executed by another of the several processors (Column 9, line 65-column 10, line 4 and configuration in figure 4, note that this an inter-processor communication configuration where communication is done on the processors' address or data bus, which allows for information to be accessed as if it were memory or a procedure otherwise known as memory mapping; additionally as specified in column 6,

lines 43-46, processor communication is for the exchange of information between the tasks which would be located in an address space of the processors' local memory).

With respect to claim 4, Kartalopoulos teaches an information processing system, which performs a real-time operation including a combination of a plurality of tasks, the system comprising: a plurality of processors (Processors 12, 14, and 16, see figure 4); means for storing (Column 2, lines 26-32) structural description information (See Matrix table in figure 1) and a plurality of programs (Column 1, lines 55- 57) describing procedures corresponding to the tasks (it is inherent that programs describe a series of procedures that correspond to a task), the structural description information indicating a relationship in input/output between the programs (Column 5, line 63-column 6, line 7 and column 6, line 43-46, note that communication and the exchange of results of one program with another indicates that there is an input/output relationship between them) and including cost information (Column 6, lines 15-30) concerning time required for executing each of the programs; means for determining an execution start timing and execution term (Column 5, line 66-column 6, line 14 and see Matrix table in figure 1) of each of a plurality of threads (it is inherent that sets of tasks are assigned to individual threads to execute) for execution of the programs based on the structural description information; and means for performing a scheduling operation (Column 6, lines 39-46 and see Matrix table of figure 1) of assigning the threads to at least one of the processors according to a result of the determining.

With respect to claim 5, Kartalopoulos teaches the information processing system according to claim 4, wherein the structural description information includes

coupling attribute information (Column 6, lines 1-7, where the coupling attribute information is the dependent task relationship represented by the Matrix table as shown in figure 1) indicative of a coupling attribute between said plurality of programs, and the system further comprises means for selecting a tightly coupled thread group from among the plurality of threads based on the coupling attribute information (Column 5, line 66-column 6 , line 3), the tightly coupled thread group including a set of tightly coupled threads running in cooperation with each other (Column 6, lines 1-6 and see Matrix table in figure 1), and means for determining several processors of the processors, to which the tightly coupled threads are to be assigned (Column 6, lines 39-44), to simultaneously execute the tightly coupled threads by the several processors (See Matrix table, as explained by Column 6, lines 39-44, note that each row corresponds to one microprocessor and as shown in the table and each column indicates simultaneous tasks to be processed in a slotted time interval), the several processors being equal in number to the tightly coupled threads (Column 6, lines 39-42).

With respect to claim 6, Kartalopoulos teaches the information processing system according to claim 5, wherein each of said plurality of processors includes a local memory (Column 2, lines 26-32), and the system further comprises means for mapping the local memory of one of the several processors, which executes one of the tightly coupled threads, in part of an effective address space of another of the tightly coupled threads executed by another of the several processors (Column 9, line 65-column 10, line 4 and configuration in figure 4, note that this an inter-processor

communication configuration where communication is done on the processors' address or data bus, which allows for information to be accessed as if it were memory or a procedure otherwise known as memory mapping; additionally as specified in column 6, lines 43-46, processor communication is for the exchange of information between the tasks which would be located in an address space of the processors' local memory).

With respect to claim 10, Kartalopoulos teaches an information processing system which, performs a real-time operation including a combination of a plurality of tasks, the system comprising: a plurality of processors (Processors 12, 14, and 16, see figure 4); a storing unit (Column 2, lines 26-32) configured to store structural description information (See Matrix table in figure 1) and a plurality of programs (Column 1, lines 55- 57) describing procedures corresponding to the tasks (it is inherent that programs describe a series of procedures that correspond to a task), the structural description information indicating a relationship in input/output between the programs (Column 5, line 63-column 6, line 7 and column 6, line 43-46, note that communication and the exchange of results of one program with another indicates that there is an input/output relationship between them) and including cost information (Column 6, lines 15-30) concerning time required for executing each of the programs; and a scheduling unit (Processor system 10, see figure 4 and column 9, lines 60-63) configured to perform a scheduling operation (Column 6, lines 39-46 and see Matrix table of figure 1) of assigning a plurality of threads (it is inherent that sets of tasks are assigned to individual threads to execute) for execution of the programs to at least one of the processors by determining an execution start timing and execution term (Column 5, line 66-column 6,

line 14 and see Matrix table in figure 1) of each of the threads based on the structural description information.

With respect to claim 11, Kartalopoulos teaches the information processing system according to claim 10, wherein the structural description information (Column 6, lines 1-7, where the coupling attribute information is the dependent task relationship represented by the Matrix table as shown in figure 1) includes coupling attribute information indicative of a coupling attribute between the programs, and the scheduling unit includes a selector to select a tightly coupled thread group from among the plurality of threads based on the coupling attribute information (Column 5, line 66-column 6 , line 3), the tightly coupled thread group including a set of tightly coupled threads running in cooperation with each other (Column 6, lines 1-6 and see Matrix table in figure 1), and a determining unit configured to determine several processors of the processors, to which the tightly coupled threads are to be assigned (Column 6, lines 39-44), to simultaneously execute the tightly coupled threads by the several processors (See Matrix table, as explained by Column 6, lines 39-44, note that each row corresponds to one microprocessor and as shown in the table and each column indicates simultaneous tasks to be processed in a slotted time interval), the several processors being equal in number to the tightly coupled threads (Column 6, lines 39-42).

With respect to claim 12, Kartalopoulos teaches the information processing system according to claim 11, wherein each of said plurality of processors includes a local memory (Column 2, lines 26-32), and the system further comprises a mapping unit (Modules 18 and 20 for the use in a Time Domain Multiplex (TDM) communication

system, see figure 4) configured to map the local memory of one of the several processors, which executes one of the tightly coupled threads, in part of an effective address space of another of the tightly coupled threads executed by another of the several processors (Column 9, line 65-column 10, line 4 and configuration in figure 4, note that this an inter-processor communication configuration where communication is done on the processors' address or data bus, which allows for information to be accessed as if it were memory, a technique otherwise known as memory mapping; additionally as specified in column 6, lines 43-46, processor communication is for the exchange of information between the tasks, which would be inherently located in an address space of the processors' local memory).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Strout, II et al (US 5,339,415) reference shows a tightly coupled multiprocessor computer system, running a plurality of multithreaded programs to run simultaneously. The Eadline (US 5,471,622) reference shows a system and method for generating lists of parallel-executable tasks and distributes them to other processors. The Schoening et al (US 6,205,465) shows execution of two or more parallel processing threads that acts on one or more sets of data, in the context of a transaction, for which parallel processing is needed. The Akashi et al (US 2002/0198924) reference teaches a scheduling function that estimates operation characteristics and then optimizes assignment of each process to a processor. The

Luick (US 7,117,389) reference teaches a multiprocessor core device that group threads, based on their dependency, to be pipelined.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwok Wing Lee whose telephone number is (571) 270-3557. The examiner can normally be reached on Mon - Thu, 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached on (571) 272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KWL

Kwok W. Lee
10/16/2007

DAVID L. ROBERTSON
SUPERVISORY PATENT EXAMINER